UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,498	10/27/2000	Ahmadreza Rofougaran	40886/CAG/B600	3857

7590 11/10/2005

Christopher C. Winslade
McAndrews, Held & Malloy
500 W. Madison Street
Suite 3400
Chicago, IL 60661

EXAMINER	
MILORD, MARCEAU	
ART UNIT	**PAPER NUMBER**
2682	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,498	ROFOUGARAN ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-20* is/are rejected.

7)☒ Claim(s) *7 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-13, 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutardja et al (US Patent No 5686867) in view of Waldie et al (US Patent No 5630215).

Regarding claim 1, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardia et al does not specifically disclose the feature of a mixer to mix the oscillator output with a second signal to produce a mixed signal; and a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

On the other hand, Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 2, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal (col. 2, lines 40-55; col. 3, lines 59-64; col. 4, line 63- col. 5, line 20).

Regarding claim 3, Sutardja et al as applied to claim 1 above differs from claim 3 in the present invention, in that Sutardja fails to disclose a bandpass filter to filter the mixed signal

before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal

Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 4, Sutardja et al as applied to claim 3 above differs from claim 4 in the present invention, in that Sutardja fails to disclose a limiter to limit the filtered mixed signal from the filter 'before being applied to the phase detector.

Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 5, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising a charge pump disposed between the phase detector and the oscillator.

Regarding claim 6, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising a loop filter disposed between the phase detector and the oscillator.

Regarding claim 8, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: a tunable oscillator having a tuning input (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardja et al does not specifically disclose the feature of a mixer coupled the oscillator; and a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

On the other hand, Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 9, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), wherein the oscillator comprises a voltage controlled oscillator (col. 2, lines 40-55; col. 3, lines 59-64).

Regarding claim 10, Sutardja et al as applied to claim 8 above differs from claim 10 in the present invention, in that Sutardja fails to disclose a bandpass filter coupled between the mixer and the first input of the phase detector.

Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 11, Sutardja et al as applied to claim 10 above differs from claim 11 in the present invention, in that Sutardja fails to disclose a limiter coupled between the bandpass filter and the first input of the phase detector.

Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 12, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising

a charge pump coupled between the phase detector output and the tuning input of the oscillator (col. 2, lines 35- 55; col. 3, lines 18-49)

Regarding claim 13, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator (col. 4, line 63- col. 5, line 33).

Regarding claim 15, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardia et al does not specifically disclose the feature of a mixer means for mixing the first signal with a second signal to produce a mixed signal; and detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

On the other hand, Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and

a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 16, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal (col. 2, lines 40-55; col. 3, lines 59-64; col. 4, line 63- col. 5, line 20).

Regarding claim 17, Sutardja et al as applied to claim 15 above differs from claim 17 in the present invention, in that Sutardja fails to disclose a filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal.

Waldie et al, from the same field of endeavor, discloses a radio that has a combined phase locked loop and an automatic frequency control loop. A mixer converts the received RF signal to an intermediate frequency signal responsive to an injection signal. The PLL locks the injection

signal to the received RF signal responsive to a difference between the IF signal and a reference signal (col. 2, lines 11-49). In addition, the IF stage uniquely comprises a mixer, an IF filter, a limiter, a phase detector, a loop filter and a voltage controlled oscillator and a frequency detector. The phase detector compares the limited IF signal and the reference signal to produce a phase error signal .The phase error signal passes through the loop filter to produce a voltage based filtered phase error signal The VCO generates the frequency based injection signal responsive to the filtered phase error signal. The processor includes a filter for filtering the frequency error signal to produce a filtered error signal; and a limit controller for limiting the filtered error signal to produce the control signal (fig. 2; col. 3, lines 5-47; col. 4, lines 1-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Waldie to the CMOS phase-lock loop circuit of Sutardja in order to provide a phase detector that can generate a phase error signal between the input signal and the output signal and detect the amplitude of the output signal.

Regarding claim 18, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising means for limiting the filtered mixed signal front the filter means before being applied to the detector means (col. 4, line 63- col. 5, line 33).

Regarding claim 19, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising means for sourcing current to the tuning means responsive to the error signal (col. 5, line 1-col. 6, line 17).

Regarding claim 20, Sutardja et al as modified discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising means for filtering the error signal from the detecting means before being applied to the tuning means (col. 3, lines 59-64; col. 4, line 63- col. 5, line 20).

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sutardja et al (US Patent No 5686867) in view of Waldie (US Patent No 5630215) as applied to claims 8, 15 above, and further in view of Hughes (US Patent No 4270206).

Regarding claim 14, Sutardja and Waldie disclose everything claimed as explained above except a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

However, Hughes discloses a phase-locked loop which includes a phase detector and a voltage controlled oscillator. The phase detector and the active portions of VCO may be provided by a single CMOS and the integrated circuit. The receiver section includes a bandpass filter amplifier means, having an input connected to receiver input and an output (col. 4, lines 2-28; col. 6, lines 1- 43; col. 7, line 41- col. 8, line 17; col. 8, lines 49-67). The input of an inverter means receives the bandpass filter amplifier output signal and provides a linear inversion at inverter, connected to second inputs respectively, of respective first and second mixer means 75 and 76 (col. 7, line 41-col. 8, line 17). Furthermore, the first mixer output has amplitude responsive to the phase difference between the signal at mixer control input and the signals at mixer inputs 75a and 75b. Similarly, second mixer 76 has an output waveform having amplitude responsive to the phase difference between the signal at control input and the signals at mixer

inputs 76a and 76b (col. 9, lines 1-34; col. 10, lines 31-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Hughes to the modified system of Waldie and Sutardja in order to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits.

Allowable Subject Matter

4. Claims 7, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1-6, 8-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 571-272-7853. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vuong B. Quochien can be reached on 571-272-7902. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARCEAU MILORD

Marceau Milord

Primary Examiner

Art Unit 2682